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PATTERSON & SHERIDAN, LLP - - APPM/TX
3040 POST OAK BOULEVARD, SUITE 1500
HOUSTON, TX 77056

EXAMINER	
MALDONADO, JULIO J	

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/756,122
Filing Date: January 13, 2004
Appellant(s): YAU ET AL.

Keith M. Tackett
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 10/09/2008 appealing from the Office action mailed 07/22/2008.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

No amendment after final has been filed.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

5817572	Chiang et al.	10-1998
6124641	Matsuura	09-2000
5718967	Hu et al.	02-1998
5970376	Chen	10-1999

Wolf et al., Silicon Processing for the VLSI Era, Volume 1: Process Technology, 1986 by Lattice Press, pages 161-174.

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 15-18, 21, 23-25, 27 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chiang ('572) in view of Matsuura (U.S. 6,124,641) and Hu et al. (U.S. 5,718,967, hereinafter Hu).

In reference to claims 15-18, 21 23-25 and 28 Chiang (Figs.15-25) teaches a method of forming interconnect structures including providing a substrate (320) having a contact (321) formed therein (Chiang, column 12, lines 52 – 63); depositing a first dielectric layer (322) on said substrate (320) (Chiang, column 13, lines 15 – 35); forming an etch stop layer (323) on said first dielectric layer (322) (Chiang, column 14, line 61 – column 15, line 4); forming a second dielectric layer (350) on said etch stop layer (323) (Chiang, column 15, lines 28 – 46); forming a photoresist layer (352) on said second dielectric layer (350) (Chiang, column 15, lines 48 – 58); and using said photoresist layer to form a contact hole (351) in said second dielectric layer (350) (Chiang, column

15, lines 59 – 62), wherein said first dielectric layer (322) and said second dielectric layer (350) may include any suitable dielectric material or materials including silicon dioxide, silicon nitride, silicon oxynitride, phosphosilicate glass, borophosphosilicate glass, fluoropolymer, parylene, polyimide, any suitable spin-on glass, or any suitable spin-on polymer (Chiang, column 13, lines 15 – 35 and column 15, lines 28 – 46), and further forming a third dielectric layer (395) over said second dielectric layer (Chiang, column 21, lines 4 – 15).

Chiang fails to disclose forming the second dielectric layer using a low dielectric constant material. However, parylene, polyimide, for example, are known low dielectric constant materials. Therefore, Chiang teach upon the claimed invention.

Chiang fails to disclose forming a low dielectric constant organosilane layer in a plasma enhanced process from a mixture comprising a methylsilane compound and an oxidizing gas, the carbon content of the low dielectric constant oxidized organosilane layer is form 1% to 50% by atomic weight.

However, Matsuura (Figs.1a-1c) teaches a method of forming a dielectric stack including the steps of depositing on a substrate (1) a plurality of layers (3, 4, 5), wherein one of the layers (4) is a low dielectric constant oxidized organosilane layer comprising carbon, wherein the low dielectric constant oxidized organosilane layer (4) is deposited in a chemical vapor deposition process from a mixture comprising methylsilane or vinylsilane, and H_2O_2, and wherein the carbon content of the low dielectric constant oxidized organosilane layer is around 18% by atomic weight (See Fig.2, for example) (Matsuura, column 4, line 17 – column 5, line 46).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Chiang and Matsuura to enable forming the low-k dielectric layers of Chiang according to the teachings of Matsuura because one of ordinary skill in the art at the time the invention was made would have been motivated to look to alternative suitable methods of forming the second dielectric layer of Chiang and art recognized suitability for an intended purpose has been recognized to be motivation to combine (MPEP 2144.07) and because this would prevent a poisoned via from being formed in a resulting insulating film (Matsuura, column 2, lines 57 - 64).

While the combination of Chiang and Matsuura discloses a carbon content of 18% atm weight, they fail to disclose wherein the carbon content of the low dielectric constant oxidized organosilane layer is from 1% to 50% by atomic weight. However, in the case where the claimed ranges “overlap or lie inside ranges disclosed by the prior art” a prima facie case of obviousness exists. MPEP 2144.05. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the carbon concentration in the dielectric layer of the combination of Chiang and Matsuura to arrive at the claimed invention.

The combined teachings of Chiang and Matsuura fail to expressly disclose wherein the chemical vapor deposition process is a plasma enhanced chemical vapor deposition process.

However, Hu teaches a method of forming oxidized organosilane layers including forming said oxidized organosilane layer using a plasma enhanced chemical vapor

deposition process using organosilicon compounds such as a silane, siloxane or a silazane (Hu, column 3, lines 18 – 61).

It would have been within the scope of one of ordinary skill in the art to combine the teachings of Chiang and Matsuura with Hu to enable the disclosed chemical vapor deposition step of Chiang and Matsuura to be performed according to the teachings of Hu because one of ordinary skill in the art would have been motivated to look to analogous art teaching alternative suitable or useful methods of performing the disclosed chemical vapor deposition step of Chiang and Matsuura and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP 2144.07.

In reference to claim 27 the combined teachings of Chiang, Matsuura and Hu teach forming the low dielectric constant oxidized organosilane layer using a plasma enhanced chemical vapor deposition process disclosed in Hu et al. to U.S. 5,298,587, "…which disclosure is incorporated herein by reference…" (Hu, column 3, lines 58 – 61).

Furthermore, the provided evidence to Hu et al. (U.S. 5,298,587), discloses wherien the deposition process is performed in the presence of RF power (Hu et al., column 2, lines 30 – 48).

Therefore, the combined teachings of Chiang, Matsuura and Hu teach the claimed limitation.

3. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chiang ('572) in view of Matsuura ('641) and Hu ('967) as applied to claims 15-18, 21 and 23-25, 27 and 28 above, and further in view of Chen (U.S. 5,970,376).

The combination of Chiang, Matsuura and Hu substantially teach the claimed invention but fail to disclose etching the low dielectric constant oxidized organosilane layer using fluorine, carbon, and oxygen ions.

However, Chen (Figs.4-7) in a related method to form interconnect structures teaches the steps of forming a low dielectric layer (32) over a substrate (30), wherein said dielectric layer has the general formula R_1-Si(OR_2)$_3$, wherein R_1 is hydrogen and R_2 is CH_3; and etching the low dielectric layer (32) using fluorine, carbon, and oxygen ions (Chen, column 4, line 66 – column 5, line 12, column 5, lines 34 – 56, column 7, lines 25 – 42, and column 8, lines 40 – 48).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Chiang, Matsuura and Hu with Chen to enable etching the dielectric layer of Chiang, Matsuura and Hu according to the teachings of Chen for the further advantage of forming vias with attenuated lateral etching of said vias (Chen, column 4, lines 39 – 63).

(10) Response to Argument

Appellants' arguments filed 10/09/2008 have been fully considered but they are not persuasive.

The appellants argue, "…The Examiner asserts, however, that Matsuura teaches the low dielectric constant oxidized organosilane layer deposited by PECVD from

methylsilane and hydrogen peroxide missing from Chiang, and that it would be obvious to combine the teachings of Matsuura with Chiang to yield the claimed invention…". In response to this argument, the office action mailed on 07/22/2008 relies upon Matsuura on a process of forming a low dielectric constant organosilane layer in a chemical vapor deposition process, not on a plasma enhanced chemical vapor deposition process, as argued by the appellants.

The appellants argue, "…Chiang does not disclose forming the layers as oxidized organosilane layers in a plasma enhanced process using a mixture comprising a methylsilane compound and an oxidizing gas. Nor does Chiang teach the carbon content of the layer…". In response to this argument, Chiang was not relied upon the argued limitation.

The appellants argue, "…Although Matsuura discloses formation of an insulating layer from methyl silane and hydrogen peroxide, and that the insulating layer contains carbon, this is not sufficient to disclose that the Matsuura film is a low dielectric constant film…". In response to this argument, one of the objectives of the invention of Matsuura is to form a film with reduced dielectric constant (Matsuura, column 2, lines 1 - 26 and lines 58 - 64). Therefore, the dielectric film of Matsuura was labeled a low dielectric constant film.

The appellants argue, "…it would not have been obvious to one of ordinary skill in the art that applying plasma to the Matsuura process would preserve any carbon in the deposited film. To deposit a film containing carbon from the Matsuura precursors, it is necessary to leave some silicon-carbon bonds undisturbed. The combined

references provide no indication that suitable conditions could be found using the plasma process of Hu that would deposit a film having silicon-carbon bonds from the Matsuura precursors…".

In response to this argument, Matsuura discloses forming a low dielectric constant oxidized organosilane layer using a chemical vapor deposition process (Matsuura, column 2, lines 57 – 64 and column 4, lines 30 – 49). Matsuura further discloses "…many modifications and variations of the present invention are possible in the light of the above teachings…" (Matsuura, column 8, lines 29 – 33). These recitations of Matsuura are seen as evidence that the process is open to other embodiments that could be used to form the low dielectric constant oxidized organosilane layer. Furthermore, Matsuura is silent to the type of energy used to form the low dielectric constant oxidized organosilane layer. Having this in mind, Hu discloses a process to form a silicon oxide layer, SiO_x, using a plasma process and organosilicon compounds, wherein the organosilicon compound includes carbon and hydrogen atoms (Hu, column 3, lines 18 - 61). Although Hu is silent in regards to the structure of the dielectric layer, there is evidence of using organosilane precursors to form oxide layers containing silicon, oxygen, carbon and hydrogen atoms.

Furthermore, the provided evidence to Wolf et al. (Silicon Processing for the VLSI Era, Volume 1: Process technology) discloses that the difference between a conventional entirely thermal chemical vapor deposition process and a plasma enhanced chemical vapor deposition process is on the type of energy applied to the system needed to perform the chemical reaction (Wolf et al., pages 166 – 167, 172).

Furthermore, entirely thermal chemical vapor deposition processes and plasma enhanced chemical vapor deposition processes are used in the formation of silicon oxides (Wolf et al., pages 168 and 171).

Since, Matsuura discloses a chemical vapor deposition process of a low dielectric constant oxidized organosilane layer and Hu discloses using forming silicon oxide layers having carbon and hydrogen atoms, and, as evidenced by Wolf, the difference between plasma enhanced chemical vapor deposition and thermal chemical vapor deposition resides on the energy applied to perform the reaction, the supplied evidence suggest that these deposition processes are interchangeable and it would have been within the scope of one of ordinary skill in the art to combine the teachings of Chiang and Matsuura with Hu to enable the disclosed chemical vapor deposition step of Chiang and Matsuura to be performed according to the teachings of Hu because one of ordinary skill in the art would have been motivated to look to analogous art teaching alternative suitable or useful methods of performing the disclosed chemical vapor deposition step of Chiang and Matsuura and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP 2144.07.

Furthermore, the fact that claimed combination of elements was “obvious to try” might show that such combination was obvious under 35 U.S.C. §103, since, if there is design need or market pressure to solve problem, and there are finite number of identified, predictable solutions, person of ordinary skill in art has good reason to pursue known options within his or her technical grasp, and if this leads to anticipated success,

it is likely product of ordinary skill and common sense, not innovation. KSR International Co. v. Teleflex Inc., 82 USPQ2d 1385 (U.S. 2007).

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

/Julio J. Maldonado/

Examiner, Art Unit 2823

Conferees:

Darren Schuberg /DS/

Matthew Smith

/Matthew S. Smith/

Supervisory Patent Examiner, Art Unit 2823

Julio J. Maldonado